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EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2181	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,874	KIM ET AL.	
	Examiner	Art Unit	
	Donna K. Mason	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☒ Claim(s) *10,18,28 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to because in Fig. 2A, the label "Fig. 2" should be changed to --Fig. 2A--. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. See 37 CFR 1.83.

2. The drawings are objected to because in Fig. 4, item 440, "MUTI-INPUT" should be changed to --MULTI-INPUT--. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. See 37 CFR 1.83.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 612. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to because in Fig. 8, the label "EDR" (between item 750 and item 810) should be changed to --EGNT--. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. See 37 CFR 1.83.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "first bus switch"

recited in claim 3 (lines 2 and 3-4) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities:

On page 5, line 8, change "CPU 422" to --CPU 222--;

On page 6, line 5, change "bus master 396" to --bus arbiter 396--;

On page 7, lines 13 and 14, "When they do not, they have to wait for another step, while the external bus 315" is recited. This is an incomplete statement as it fails to address what the external bus 315 does while the functional blocks wait for another step;

On page 11, line 9, insert --it-- between "that receives".

Appropriate correction is required. See 37 CFR 1.71.

Claim Objections

7. Claims 10, 18, 28, and 31 are objected to because of the following informalities:

8. In claim 10, line 1, insert ":" after "includes".

9. In claim 18, line 4, it is recommended that "they" be changed to --the received requests--.

10. In claim 18, line 8, delete "that" after "bus".

11. In claim 28, line 3, change "a" to --an-- before "on-chip".

12. In claim 31, line 10, delete "that" after "bus".

13. Appropriate correction is required. See 37 CFR 1.75.

Claim Rejections - 35 USC § 112

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 3-20 and 23-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

16. Claim 3 recites "a first bus switch" in lines 2 and 3-4. However, in the present application, applicant has stated that "[a]n additional, auxiliary system bus APB 516, . . . , is connected to main system bus 410 through a main bridge block 518," (page 12, lines 5-6) and this statement indicates that the invention is different from what is defined in the claim(s) because as shown in Fig. 5, a main bridge block 518 connects the system bus to the auxiliary system bus instead of a "first bus switch" connecting the two busses, as claimed. Furthermore, as shown in Fig. 6, only one bus switch is illustrated (AHB switch), and that bus switch does not connect the system bus to the auxiliary bus.

To the contrary, the main bridge block 518 connects the system bus to the auxiliary system bus, while the bus switch divides the left system bus and the right system bus (page 12, lines 18-29). For examination purposes, "a first bus switch" has been interpreted as being a bridge as shown in Figs. 5 and 6, item 518.

17. Claim 4 recites the limitation "a second bus switch" in line 2. However, there is no prior reference to "a first bus switch" in independent claim 1. For examination purposes, "a second bus switch" has been interpreted as being --a bus switch--, as illustrated in Fig. 6.

18. Claim 5 recites the limitation "a third path" in line 5. However, there is no prior reference to either a "first path" or a "second path". For examination purposes, "a third path" has been interpreted as --a path-- distinct from the system bus and external bus.

19. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the receipt of the third output from the priority scheduler 720 by the request decoder 710 (see Fig. 8). Claim 12, recites "the third output is first received and decoded by *the system bus master selector*" (emphasis added) in line 2. However, it appears from Fig. 8 that the third output is first received and decoded by the request decoder 710 -- not by the system bus master selector, as claimed. For examination purposes, claim 12 has been interpreted with reference to Fig. 8, such that the request decoder receives and decodes the third output from the priority scheduler.

20. Claim 18 recites the limitation "the buses" in line 5. There is insufficient antecedent basis for this limitation in the claim.

21. Claim 18 recites "whether they would use one of a system bus of an on-chip system, an external bus of the system, and both the buses" in lines 4-5. It appears that applicant is attempting to use an alternative expression, where a system bus, an external bus, or both the system bus and the external bus are presented as alternatives. However, the use of "and" before "both the buses" creates uncertainty or ambiguity with respect to the question of scope or clarity of the claim. For examination purposes, this limitation has been interpreted as --whether the received requests would use one of a system bus of an on-chip system, an external bus of the system, or both the system bus and the external bus--.

22. Claim 23 recites the limitation "the buses" in line 7. There is insufficient antecedent basis for this limitation in the claim.

23. Claim 23 recites "whether they would use one of the system bus, the external bus, and both the buses" in lines 6-7. It appears that applicant is attempting to use an alternative expression, where a system bus, an external bus, or both the system bus and the external bus are presented as alternatives. However, the use of "and" before "both the buses" creates uncertainty or ambiguity with respect to the question of scope or clarity of the claim. For examination purposes, this limitation has been interpreted as --whether the received requests would use one of a system bus, an external bus, or both the system bus and the external bus--.

24. Claim 26 recites the limitation "the auxiliary system bus" in line 6. There is insufficient antecedent basis for this limitation in the claim.

25. Claim 27 recites the limitation "the auxiliary system bus" in line 2. There is insufficient antecedent basis for this limitation in the claim.

26. Claim 28 recites the limitation "a second on-chip functional block" in lines 1-2. However, there is no prior reference to "a first on-chip functional block". For examination purposes, "a second on-chip functional block" has been interpreted as --an on-chip functional block--.

27. Claim 31 recites the limitation "the buses" in line 7. There is insufficient antecedent basis for this limitation in the claim.

28. Claim 31 recites "whether they would use one of the system bus, the external bus, and both the buses" in lines 6-7. It appears that applicant is attempting to use an alternative expression, where the system bus, the external bus, or both the system bus and the external bus are presented as alternatives. However, the use of "and" before "both the buses" creates uncertainty or ambiguity with respect to the question of scope or clarity of the claim. For examination purposes, this limitation has been interpreted as --whether the received requests would use one of the system bus, the external bus, or both the system bus and the external bus--.

29. Claim 34 recites the limitation "a second on-chip functional block" in line 2. However, there is no prior reference to "a first on-chip functional block". For examination purposes, "a second on-chip functional block" has been interpreted as --an on-chip functional block--.

30. Claim 34 recites the limitation "control *the only* external bus" (emphasis added) in line 8. However, upon review of the disclosure, it appears that Applicant intends this limitation to read --control *only the* external bus-- (emphasis added). For examination purposes, the latter interpretation has been used.

31. Claims 6-11, 13-17, 19, 20, 24, 25, 29, 30, 32, 33, and 35 inherit the deficiencies of their respective independent claims.

Claim Rejections - 35 USC § 102

32. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

33. Claims 1, 5, 9, 23, 24, and 28-35 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,438,635 to Date, et al. ("Date").

With regard to independent claim 1, Date discloses a semiconductor device including a chip (column 6, lines 18-24), a plurality of first blocks on the chip (Fig. 35, items 402 and bus masters 1, 2, 3, and 4), a system bus on the chip coupled with the first blocks (Fig. 35, item 404), an external bus (Fig. 35, item 405) for coupling a dual one of the first blocks (Fig. 35, item 402) to a plurality of second blocks (Fig. 54) external to the chip. Dale also discloses a single on-chip multi-jurisdictional arbiter (Fig.

35, item 406) adapted to receive requests for ownership of the system and of the external bus (column 28, lines 5-12), to rank all the received requests according to a programmable priority schedule (column 28, lines 1-4), to transmit a first grant signal to the dual first block regarding a first ownership of the external bus (column 28, lines 15-38), and to transmit a second grant signal regarding a second ownership of the system bus to another one of the first blocks that is concurrent with the first ownership (column 27, lines 25-29).

With regard to independent claim 5, Date discloses a device including a semiconductor chip (column 6, lines 18-24), a system bus on the chip (Fig. 356, item 404), an external bus (Fig. 35, item 405), a path distinct from the system bus and the external bus (Fig. 35, path between items 3501 and 403), and a plurality of first blocks on the chip coupled directly with the system bus (*see, e.g.*, Fig. 35, item 402 and bus masters 1, 2, 3, and 4). Date also discloses a device where at least one of the first blocks is an external memory controller (Fig. 35, item 403) coupled to the external bus and adapted to control at least one memory device that is external to the chip, and another one of the first blocks is a multi-jurisdictional multi-channel general direct memory access block (Fig. 35, item 3501) that is coupled with the external memory controller via the third path.

With regard to dependent claim 9, Date discloses the device, further including an on-chip multi-jurisdictional arbiter (Fig. 35, item 406) adapted to transmit a first grant signal to one of the first blocks regarding a first ownership of the system bus and to transmit a second grant signal to the external memory device regarding a second

ownership of the external bus that is concurrent with the first ownership (column 27, lines 25-29).

With regard to independent claim 23, Date discloses a method for a semiconductor chip having a plurality of on-chip functional blocks (Fig. 35, items 402 and bus masters 1, 2, 3, and 4), at least one on-chip system bus (Fig. 35, item 404) for connecting at least some of the blocks, and an external bus (Fig. 35, item 405) for at least one of the functional blocks to exchange data with off-chip devices, the method including the steps of receiving a plurality of requests (column 30, lines 19-21), characterizing the received requests in terms of whether the requests would use one of a system bus, an external bus, or both the system bus and the external bus (column 29, lines 66-67 to column 30, lines 1-5), selecting a first one of the requests (column 30, lines 21-23), identifying the buses that would be idle if the first request were performed (column 30, lines 30-42), selecting a second one of the requests that can be performed by at least one of the system bus and the external bus that would be idle if the first request were performed (column 30, lines 30-42), and granting the second request concurrently with granting the first request (column 27, lines 25-29).

With regard to dependent claim 24, Date further discloses the step of assigning respective non-hierarchical priorities to all the requests by a single chip multi-jurisdictional arbiter (column 30, lines 6-13), where the first request is the one with a top one of the priorities.

With regard to independent claim 28, Date discloses a method for a semiconductor chip (column 6, lines 18-24) having an on-chip CPU block (Fig. 35, item

401), an on-chip functional block (Fig. 35, item 402), at least one on-chip system bus (Fig. 35, item 404) for connecting the on-chip blocks, an on-chip DRAM refresh controller (Fig. 35, item 403), and an external bus (Fig. 35, item 404), the method including the steps of receiving a plurality of requests, a first one of which being from the DRAM refresh controller (column 30, lines 19-21), examining whether a second one of the remaining requests is for using only the system bus (column 29, lines 66-67 to column 30, lines 1-5), and if so, granting the first and second requests to be performed concurrently (column 30, lines 30-42).

With regard to dependent claim 29, Date further discloses the steps of assigning priorities to the requests (column 30, lines 6-13), selecting a request having a second one of the priorities (column, lines 6-13), and determining whether the selected request can be the second request (column 30, lines 6-13).

With regard to dependent claim 30, Date further discloses the step of determining whether a request having a third one of the priorities can be the second request, if the request having the second one of the priorities cannot be the second request (column 30, lines 6-13).

With regard to independent claim 31, Date discloses a method for a semiconductor chip (column 6, lines 18-24) having a plurality of functional blocks (Fig. 35, items 402 and bus masters 1, 2, 3, and 4), at least one on-chip bus for connecting at least some of the blocks (Fig. 35, item 404), and an external bus (Fig. 35, item 405) for at least one of the functional blocks to exchange data with off-chip devices, the method including the steps of receiving a plurality of requests (column 30, lines 19-21),

characterizing the received requests in terms of whether the requests would use one of the system bus, the external bus, or both the system bus and the external bus (column 29, lines 66-67 to column 30, lines 1-5), assigning priorities to the requests according to preset rankings (column 30, lines 6-13), selecting a first one of the requests having a top one of the priorities (column 30, lines 21-23), determining whether at least one of the system bus and external bus would be idle if the first request were granted, and if so, selecting a second one of the requests that can be performed by at least one of the would-be idle buses, and then granting concurrently the first request and the second request (column 30, lines 30-42).

With regard to dependent claims 32 and 33, Date further discloses the steps of determining whether a request having a second one of the priorities can be the second request (column 30, lines 6-13), and if the request having the second one of the priorities can not be the second request, determining whether a request having a third one of the priorities can be the second request (column 30, lines 6-13).

With regard to independent claim 34, Date discloses a method for a semiconductor chip (column 6, lines 18-24) having an on-chip multi-jurisdictional multi-channel general direct memory access (mJmCGDMA) block (Fig. 35, item ____), a second on-chip functional block (Fig. 35, item ____), at least one on-chip system bus (Fig. 35, item 404) for connecting the on-chip blocks, and an external bus (Fig. 35, item 405) for the mJmCGDMA block to exchange data with an off-chip device, the method including the steps of granting a request by the mJmCGDMA block to control only the system bus in a first cycle (column 29, lines 60-65), and then granting a request by the

mJmCGDMA block to control only the external bus in a second cycle subsequent to the first cycle (column 30, lines 19-29).

With regard to dependent claim 35, Date further discloses the step of granting a request by the mJmCGDMA block to control both the system bus and the external bus concurrently in a third cycle subsequent to the second cycle (column 30, lines 52-56).

Therefore, Date reads on the invention as claimed.

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 2 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Date in view of U.S. Patent No. 6,046,952 to Novak, et al. ("Novak").

As described above with regard to the anticipation rejection, Date discloses all the features of independent claims 1 and 5 and dependent claim 9. With regard to dependent claims 2, 10 and 11, Date does not expressly disclose the device, where the arbiter includes a request decoder, a priority scheduler, a system bus master selector, an external bus master selector, and a system bus slave selector.

Regarding claims 2 and 10, Novak discloses an arbiter (Fig. 2, item 220) that includes a request decoder (Fig. 2, item 340) to receive a request signal from one of an external memory device and one of the first blocks, a priority scheduler (Fig. 2, item

310) to receive an output of the request decoder, a system bus master selector (Fig. 2, item 320) to receive a first output of the priority scheduler containing data about a first top priority and further adapted to transmit the first grant signal responsive to the first top priority, and an external bus master selector (Fig. 2, item 320) to receive a second output of the priority scheduler containing data about a second top priority and further adapted to transmit the second grant signal responsive to the second top priority.

With regard to dependent claim 11, Novak discloses a system bus slave selector (Fig. 2, item 320) to transmit a select signal to one of the first blocks responsive to a third output originating from the priority scheduler.

With regard to dependent claim 12, Date fails to disclose the device where the third output is first received and decoded by the request decoder, and the system bus slave selector is adapted to receive from the system bus master selector a corresponding signal responsive to the third output. Novak discloses the device where the third output is first received and decoded by the request decoder (Fig. 2, item 340), and the system bus slave selector is adapted to receive from the system bus master selector a corresponding signal responsive to the third output (Fig. 2, item 400).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the arbiter of Novak with Date. The suggestion or motivation for doing so would have been to optimize bus control mechanisms in the system (see column 1, lines 58-63).

Therefore, it would have been obvious to combine Novak with Date to obtain the invention as specified in claims 2 and 10-12.

36. Claim 3, 4, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Date in view of U.S. Patent No. 6,081,863 to Kelley, et al. ("Kelley").

As described above with regard to the anticipation rejection, Date discloses all the features of independent claims 1 and 23. With regard to dependent claim 3, Date does not expressly disclose a first bus switch (interpreted as a main bridge), an auxiliary system bus, and a plurality of third blocks coupled with the auxiliary system bus, where the arbiter is adapted to transmit a third grant signal to one of the third blocks regarding a third ownership of the auxiliary system bus that is to be concurrent with the first ownership.

Kelley discloses a first bus switch (interpreted as a main bridge) (Fig. 3, item 76), an auxiliary system bus (Fig. 3, item 84) on the chip coupled to the system bus through the first bus switch (main bridge), and a plurality of third blocks (Fig. 3, items 98) on the chip coupled with the auxiliary system bus, where the arbiter (Fig. 3, item 102) is adapted to transmit a third grant signal to one of the third blocks regarding a third ownership of the auxiliary system bus that is to be concurrent with the first ownership.

With regard to dependent claim 4, Date does not disclose the device where the system bus is split into a left portion and a right portion separated by a bus switch. Kelley discloses a device where the system bus (Fig. 3, item 90) is split into a left portion (Fig. 3, BUS B1) and a right portion (Fig. 3, BUS B2) separated by a second bus switch (Fig. 3, item 86), and the arbiter (Fig. 3, item 101) is adapted to transmit a control signal to the second bus switch.

With regard to dependent claim 25, Date further discloses the step of identifying all buses on the chip that would be idle if the first request and the second request were performed concurrently (column 30, lines 30-51). Date does not expressly disclose the steps of selecting a third one of the requests that can be performed by an auxiliary system bus on the chip which would be idle if the first request and the second request were performed concurrently, and granting the third request concurrently with granting the first request.

Kelley discloses the steps of selecting a third one of the requests that can be performed by an auxiliary system bus on the chip which would be idle if the first request and the second request were performed concurrently (column 4, lines 37-47), and granting the third request concurrently with granting the first request (column 4, lines 47-59).

With regard to dependent claim 26, Date further discloses the steps of transferring a first set of data through the system bus pursuant to the granted first request (column 30, lines 43-46), transferring a second set of data through the external bus pursuant to the granted second request concurrently with transferring the first set of data (column 30, lines 46-51). Date does not expressly disclose the step of transferring a third set of data through the auxiliary system bus pursuant to the granted third request concurrently with transferring the first set of data.

Kelley discloses the step of transferring a third set of data through the auxiliary system bus pursuant to the granted third request concurrently with transferring the first set of data (column 5, lines 23-47).

With regard to dependent claim 27, Date does not expressly discloses the step of transferring a single set of data through the auxiliary system bus, the system bus, and the external bus pursuant to the granted first, second and third requests. Kelley discloses the step of transferring a single set of data through the auxiliary system bus, the system bus, and the external bus pursuant to the granted first, second and third requests (column 5, lines 23-47).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the device of Kelley with Date. The suggestion or motivation for doing so would have been to provide expansion capabilities in a multi-bus system (column 1, lines 57-67).

Therefore, it would have been obvious to combine Kelley with Date to obtain the invention as specified in claim 3, 4, and 25-27.

37. Claim 6-8 and 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Date in view over U.S. Patent No. 6,003,116 to Morita, et al. ("Morita").

As described above with regard to the anticipation rejection, Date discloses all the features of independent claim 5 and dependent claim 9. With regard to dependent claims 6 and 13, Date does not expressly disclose the device where the external memory controller includes an external bus controller, an address and control multiplexer, a write data multiplexer, and a read data demultiplexer.

Morita discloses an external bus controller (Fig. 2, item 421a) to control the external bus, an address and control multiplexer (Fig. 2, item 427a) adapted to receive

address and control inputs from both the system bus and the multi-jurisditional multi-channel general direct memory access block, and adapted to transfer one of the received address and control inputs to the external bus controller, a write data multiplexer (Fig. 2, item 429a) adapted to receive data inputs from both the system bus and the multi-jurisditional multi-channel general direct memory access block, and adapted to transfer one of the received data inputs to the external bus controller, and a read data demultiplexer (Fig. 2, item 428a) adapted to receive data inputs from the external bus controller, and adapted to transfer the received data inputs to one of the system bus and the chip multi-jurisditional multi-channel direct memory access block.

With regard to dependent claim 7 and 14, Date does not disclose a device where the address and control multiplexer, the write data multiplexer, and the read data demultiplexer are controlled by inputs from the external bus controller. Morita discloses the device where the address and control multiplexer (Fig. 2, item 427a), the write data multiplexer (Fig. 2, item 429a), and the read data demultiplexer (Fig. 2, item 428a) are controlled by inputs from the external bus controller (Fig. 2, item 421a).

With regard to dependent claim 8 and 15, Date does not disclose the device, further including at least one buffer coupled between the external bus controller and the external bus. Morita discloses the device, further including at least one buffer (Fig. 2, items 431a, 432a, and 433a) coupled between the external bus controller and the external bus.

With regard to dependent claim 16 and 17, Date discloses an arbiter for controlling the external bus as a master. Date does not expressly disclose an external

bus controller. Morita discloses an external bus controller (Fig. 2, item 421a) adapted to receive an external bus grant signal from an arbiter for controlling the external bus as a master, and adapted to receive a select signal from the arbiter for being controlled as a slave.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the external memory controller of Morita with Date. The suggestion or motivation for doing so would have been to provide control of the external bus.

Therefore, it would have been obvious to combine Morita with Date to obtain the invention as specified in claims 6-8 and 13-17.

38. Claims 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Date in view of U.S. Patent No. 6,195,723 to Neal, et al. ("Neal").

With regard to independent claim 18, Date discloses an article including instructions (column 29, lines 66-67 to column 30, lines 1-5), that when executed by at least one device, result in receiving a plurality of requests (column 30, lines 19-21), characterizing the received requests in terms of whether the requests would use one of a system bus of an on-chip system, an external bus of the system, or both the system bus and the external bus (column 29, lines 66-67 to column 30, lines 1-5), assigning priorities to the requests according to preset rankings (column 30, lines 6-13), selecting a first one of the requests having a top one of the priorities (column 30, lines 21-23), determining whether at least one of the system bus and external bus that would be idle

if the first request were granted, and if so, selecting a second one of the requests that can be performed by at least one of the would-be idle buses, and then granting concurrently the first request and the second request (column 30, lines 30-42).

With regard to dependent claims 19 and 20, Date discloses the article where the instructions further result in determining whether a request having a second one of the priorities can be the second request (column 30, lines 6-13), and if the request having the second one of the priorities can not be the second request, determining whether a request having a third one of the priorities can be the second request (column 30, lines 6-13).

With regard to independent claim 21, Date discloses an article including instructions (column 29, lines 66-67 to column 30, lines 1-5), that when executed by at least one device, result in granting a request by an on-chip multi-jurisdictional multi-channel general direct memory access (mJmCGDMA) block to control only a system bus in an on-chip system (column 29, lines 60-65), and then granting a request by the mJmCGDMA block to control only an external bus in an off-chip system (column 30, lines 19-29).

With regard to dependent claim 22, Date discloses the article where the instructions further result in granting a request by the mJmCGDMA block to control both the system bus and the external bus concurrently (column 30, lines 52-56).

Date does not expressly disclose a storage medium having stored thereon the instructions, as described in independent claims 18 and 21. As shown in Fig. 2 (item 78), Neal discloses a storage medium having stored thereon the instructions. At the

time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the storage medium of Neal with Date. The suggestion or motivation for doing so would have been to provide a removable read-only storage medium for the instructions, thereby preventing users from overwriting the instructions (column 5, lines 38-41).

Therefore, it would have been obvious to combine Neal with Date to obtain the invention as specified in claims 18-22.

Conclusion

39. A shortened statutory period for reply is set to expire THREE MONTHS from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this communication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (703) 305-1887. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

XUAN M. THAI
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DKM